Q.P. Code: 16EC5508 **R16**

Reg. No. | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

M.Tech I Year II Semester (R16) Regular Examinations June 2016

SUBJECT NAME: HARDWARE SOFTWARE CO-DESIGN

Time: 3 hours Max. Marks:60

(Answer all Five Units 5 X 12 =60 Marks)

UNIT-I

1	a.	Explain about hardware – software partitioning.	6M
	b.	Discuss about performance analysis in distributed system co synthesis	6M
		OR	
2	a.	What is meant by software co-design? Explain the co-design models.	6M
	b.	List the different blocks in VLIW architecture and explain. ..	6M
		UNIT-II	
3	a.	Explain in detail about prototyping and emulation techniques.	7M
	b.	Discuss about prototyping and emulation environments..	5M
		OR	
4	a.	Explain the architecture of control dominated system..	7M
	b.	Discuss about mixed system..	5M
		UNIT-III	
5	a.	Explain the co-design computational model	6M
	b.	Distinguish between design specialization and verification.	6M
		OR	
6	a.	Explain principal set of design tools for embedded processor system	7M
	b.	List the practical considerations in a compiler development environment.	5M
		UNIT-IV	
7	a.	Write short notes on interfacing component..	7M
	b.	What is meant by coordinating concurrent computations? Explain	5M
		OR	
8	a.	Explain co-design computational model.	7M
	b.	Discuss in detail about design verification co-design.	5M
		UNIT-V	
9	a.	What are the new trends in COSMA system?.	7M
	b.	Discuss how design representation for system level synthesis is done.	5M
		OR	
10	a.	Discuss the multi-language co-simulation lycos system	7M
	b.	What are the different heterogeneous specifications?	5M

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